REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-21 in the application. In previous responses, the Applicant amended Claims 1-3, 5-6, 14-16, 18, and 21 and cancelled Claims 19-20 without prejudice or disclaimer. In the present response, the Applicant has amended Claims 1, 8, 11, 18 and 21 and canceled Claim 7 without prejudice or disclaimer. Accordingly, Claims 1-6, 8-18 and 21 are currently pending in the application.

I. Formal Matters and Objections

The Examiner has objected to Claim 21 as containing an informality; namely, a typographical error. In response, the Applicant has amended Claim 21 to correct this inadvertent error and appreciates the Examiner's diligence in finding and bringing this error to his attention.

II. Rejection of Claims 1-7, 11, 14-18 and 21 under 35 U.S.C. §103

The Examiner has rejected Claims 1-7, 11, 14-18 and 21 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,922,065 to Hull ("Hull"), in view of an article entitled, "Unifying FPGAs and SIMD Arrays" by Bolotski, *et al.* ("Bolotski") and further in view of an article entitled, "Computer Architecture: A Quantitative Approach" by Hennessy ("Hennessy"). The Applicant respectfully disagrees as argued below.

The Examiner has accepted the arguments submitted in the previous response that a system of Hull (US 5,922,065) in view of Bolotski ("Unifying FPGAs and SIMD Arrays") does not disclose "control instructions having a control bit width" and "data processing instructions having a data processing bit width wider than the control bit width". Indeed in Hull, all of the instructions have the

same bit width (*e.g.*, 41 bits as stated in column 3, lines 61 to 63). However, the Examiner now newly cites Hennessy ("Computer Architecture: A Quantitative Approach") and states that Claims 1-7, 11, 14-18 and 21 are unpatentable over Hull in view of Bolotski, further in view of Hennessy.

The Examiner states that "Hull does note in column 1, lines 15 to 23 that previous instruction sets used variable-length architecture, but Hull happens to be designed for a RISC machine". However, this does not appear to be the full picture. This section of Hull describes that early processors used variable length encoding in which different instructions were encoded with different bit lengths, but that this encoding method was improved on by reduced instruction set computing (RISC) machines in which all fields are uniformly encoded, with every instruction having a fixed length (e.g. 32 bits). This directly teaches away from encoding different instructions with different bit lengths. Therefore, even if a skilled person was aware of variable length instructions, they would not look to modify the system of Hull to include such variable length instructions since such variable length instructions are described in Hull as being less desirable than fixed length instructions. It is therefore submitted that a combination of Hull with any prior art document disclosing variable length instructions (be it Hennessy or another document) would not make the features of claim 1 obvious, because a skilled person is taught against modifying the system of Hull to include variable length instructions.

It is therefore submitted that the combination of features in claim 1 of the "control instructions having a control bit width" and "data processing instructions having a data processing bit width wider than the control bit width", would not be obvious from the cited prior art.

The above arguments notwithstanding claim 1 is not obvious in view of the cited prior art for the following reasons, also.

As the Examiner states, Hennessy discloses variable length instructions. Figure D.8 on page D-13 in Hennessy shows different instructions having different lengths. However, Hennessy does not appear to refer to instruction packets comprising a plurality of instructions of different lengths. The 'bundles' (30) shown in Figure 3 of Hull contain three 41-bit instruction slots, a 4-bit template field and a stop bit. The template field specifies the mapping of instruction slots to execution unit types. As stated in column 3, lines 61 to 63 all instructions in the instruction set of the processor are 41 bits in length.

Neither Hull nor Hennessy disclose instruction packets comprising different types of instructions having different bit lengths, whilst the instruction packets all have equal bit lengths. Using variable length instructions in the system of Hull would result in variable length instruction packets, *i.e.*, the instruction packets would not all have equal bit lengths.

It is therefore submitted that none of the cited prior art documents in combination or otherwise disclose or suggest the combination of features in claim 1 including: "instruction packets comprising a plurality of only control instructions, the control instructions having a control bit width," "instructions packets comprising a plurality of instructions comprising at least one data processing instruction, the data processing instructions having a data processing bit width wider than the control bit width" and "the instruction packets being all of equal bit length." For at least this reason it is submitted that claim 1 is not obvious in view of the cited prior art documents.

Furthermore, claim 1 now explicitly states that the decode unit passes control instructions having the control bit width to a control processing channel and passes data processing instructions having the data processing bit width wider than the control bit width to a data processing channel. The cited prior art appears to fail to disclose or suggest to pass instructions of different bit widths to

different processing channels. This novel feature advantageously allows the different channels to be adapted and optimized to handling instructions of different sizes. For at least this reason it is submitted that claim 1 is not obvious in view of the cited prior art documents.

It is therefore submitted that there are at least three reasons why claim 1 is not obvious in view of the cited prior art as described above. Independent Claims 18 and 21 are not obvious in view of the cited prior art for the same reasons as those given above in relation to claim 1. Thus, the cited prior art fails to provide a *prima facie* case of obviousness of independent Claims 1, 18 and 21 and Claims dependent thereon. The Applicant therefore respectfully requests the Examiner withdraw the §103(a) rejection of Claims 1-7, 11, 14-18 and 21 and allow issuance thereof.

III. Rejection of Claims 8-10, 12 and 13 under 35 U.S.C. §103

The Examiner has rejected Claims 8-10, 12, and 13 under 35 U.S.C. §103(a) as being unpatentable over Hull, Hennessy, and Bolotski in further view of *In re Rose*. As noted above, the cited combination of Hull, Hennessy and Bolotski does not provide a *prima facie* case of obviousness of independent Claim 1. *In re Rose* has not been cited to cure the above noted deficiencies of Hull, Hennessy and Bolotski but to address the additional limitations of dependent Claims 8-10, 12 and 13. The cited combination of Hull, Hennessy, Bolotski and *In re Rose*, therefore, does not provide a *prima facie* case of obviousness of independent Claim 1 and Claims 8-10, 12 and 13 which depend thereon. The Applicant, therefore, respectfully requests the Examiner withdraw the §103(a) rejection of Claims 8-10, 12 and 13 and allow issuance thereof.

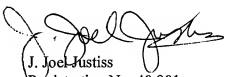
IV. Conclusion

In view of the foregoing amendment and remarks, the Applicant sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-6, 8-18 and 21.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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